Billy Koech and Nicolas Weinger

CS 141: Computing Hardware

Lab 4 Part 2 : MIPS Datapath (I-Types)

Testing methodology

The MIPS data path is implemented to support R types (except for jr which will be implemented later along with J types) and I types. The following blocks are implemented as modules and instantiated in the MIPS core module:

1. Control
2. ALU control
3. ALU
4. PC Register
5. Register File
6. IorD mux
7. IR register
8. MDR register
9. RegDst mux
10. MemtoReg mux
11. A register
12. B register
13. ALUSrcA 3 to 1 mux
14. ALUSrcB 5 to 1 mux
15. PCSource 3 to 1 mux
16. ALUout register

The Control FSM module is tested by creating a testbench that resets the FSM and runs it for about 100 clock cycles. The waveform of the enable pins (*IRWrite, MemWrite RegWrite, PCWriteCond*) and select pins (*IorD, ALUSrcA, ALUSrcB, ALUOp, PCSource, RegDst,*

*MemtoReg*) are then observed in each state and checked for consistency with the MIPS R-Type FSM diagram.

In order to test for functionality of the entire data path for I–types we convert assembly code to machine code and load it into the instruction memory. Below is how we test the required I–types:

nor $t0, $t0, $t0 # load 1s into t0

addi $t1, $t0, -15 # 4 LSBs=0

ori $t2, $t1, 7 # one zero at 4th pos

xori $t3, $t2, 8 # all 1s

slti $t4, $0, 1 # lsb = 1

sw $t0, 16($0) # DMEM 0x4 has all 1s

sw $t1 4($0) # DMEM 0x1 has all 1s

lw $t5, 4($0) # t5 has all 1s

We then view the waveform of the 32 registers in the Register File and check whether they hold the values given in the comments in the above code. We found that they did.